REMARKS

This paper is responsive to an Office Action dated July 26, 2005. Prior to this response, claims 16-26 were pending. After amending claims 16, 20-23, and 25, canceling claims 18-19, and adding claims 27-28, claims 16-17 and 20-28 remain pending.

Section 3 of the Office Action states that claims 16-17, 22, and 25-26 have been rejected under 35 U.S.C. 102(b) as anticipated by Halliyal (US 6,451,641). The Office Action states that Halliyal describes all the steps of claim 16, including the step of forming a single charge trapping layer, in Step S502 (Fig. 5).

To further clarify the claimed invention, claim 16 has been amended to recite the steps of depositing a high-k material, exposing the high-k material to an ionized species; and, in response to the ionized species exposure, inducing charge trapping centers in the high-k dielectric material. Halliyal does not describe the steps of exposing a high-k dielectric material to an ionized species, or inducing charge trapping centers in the high-k dielectric material as a result of the exposure. Since Halliyal does not explicitly describe every limitation of claim 16, he cannot anticipate. Claims 17, 22, and 25-26, dependent from claim 16, enjoy the same distinctions from the cited prior art and the Applicant requests that the rejection be removed.

In Section 11 of the Office Action claims 18, 19, and 21 have been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, in view of Tiwari (US 2004/0108537). The Office Action acknowledges that Halliyal does not describe either a plasma exposure or

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ion implantation step, to improve charge trapping characteristics. The Office Action also states that Tiwari suggests ion implantation or plasma exposure to incorporate charge trapping centers into Halliyal's high-k dielectric. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

As noted in the Applicant's specification, one purpose of the claimed invention is to replace the conventional oxide-nitride-oxide (ONO) gate multilayer stack, as used in a NROM or MONOS memory device, with a single layer of high-k dielectric that has been plasma treated to enhance its charge trapping characteristics (page 2, ln. 23 through page 3, ln. 25). More specifically, the specification notes that one of the primary problems associated with an ONO stack is that silicon nitride is not an ideal charge trapping material (page 3, ln. 15-21).

Halliyal generally describes a MOS transistor made with a high-k dielectric (Abstract). The novelty of Halliyal's invention appears to be a method of forming a polySi gate electrode that does not "reduce" the

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underlying high-k dielectric gate insulator (col. 5, ln. 27-46). Halliyal mentions that his device may be used as a FET in an EEPROM memory. However, Halliyal does not describe either a NROM or MONOS memory device, or any kind of transistor that operates on a charge trapping or floating gate principle. More particularly, Halliyal does not describe a device where charge can be trapped in a gate stack.

Tiwari describes a memory device that includes a charge trapping region formed between a substrate and an active Si layer (Abstract). Tiwari's charge trapping region is shown with specificity in Fig. 15d, as an oxide-nitride-oxide (ONO) multilayer. Tiwari states that charge trapping centers can be formed in the silicon nitride layer 322 by ion implantation or plasma implantation [0065].

With respect to the first *prima facie* requirement, there must be some suggestion in the Tiwari reference to modify Halliyal in a manner that makes the claimed invention obvious. The Office Action states that Tiwari suggests ion or plasma implantation, "to incorporate trapping centers into Halliyal's trapping layer". However, the motivation to combine references cannot be based upon a retrospective desire to turn the Halliyal invention into a memory device. Halliyal does not describe a "trapping layer" that can be modified. That is, Halliyal never mentions that his high-k dielectric can be used for charge trapping, or that his MOSFET can be used as a memory transistor. Even more critical, Tiwari never mentions that his process is applicable to high-k dielectric materials. Tiwari only describes ion implantation as performed on a silicon nitride material (silicon nitride is a low-k dielectric – see Halliyal at col. 3, ln. 13-19). Therefore, there is no support for the contention that Halliyal's dielectric can be modified to perform a completely different

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(memory) function, based upon a process (implantation of a high-k dielectric) that is not even discussed in the Tiwari reference.

Considered from the perspective of the second *prima facie* requirement, even if an expert were given the Halliyal and Tiwari inventions as a foundation, there is no reasonable expectation that this expert could derive the claimed invention, since the claimed invention describes an invention where an ion implanted high-k dielectric is used as a gate stack charge trapping layer in a memory device.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. As noted above, Applicant's claim 16 recites a memory device formed through the steps of exposing a high-k material to an ionized species; and, in response to the ionized species exposure, inducing charge trapping centers in the high-k dielectric material. Neither of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that that make these limitations obvious. Claim 21, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 15 of the Office Action, claim 20 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, and further in view of Afanas'ev. The Office Action acknowledges that Halliyal and Tiwari do not describe oxygen, nitrogen, and hydrogen plasmas. The Office Actions states that "Afanas'ev teaches that nitrogen increases trapping centers in Halliyal's trapping layer and, therefore can be used to diminish the degrading impact of hole trapping". This rejection is traversed as follows.

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In his **Conclusions**, Afanas'ev states that nitrogen impurities can be used to enhance electron trapping in Al2O3, ZrO2, and HfO2 materials. However, Afanas'ev never describes any type of implantation process. More specifically, Afanas'ev only describes as-deposited nitrogen-containing films (Abstract). Therefore, it is not evident how Afanas'ev study of as-deposited impurities in high-k dielectrics suggest any modifications to Tiwari's ion implantation of a low-k dielectric film. Likewise, there appears to be no suggestion to combine Afanas'ev study of as-deposited impurities in high-k dielectrics with a process (Halliyal) that protects a high-k dielectric material from reduction when an overlying polySi gate electrode is formed.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. As noted above, Applicant's claim 16 recites a memory device formed through the steps of exposing a high-k material to an ionized species; and, in response to the ionized species exposure, inducing charge trapping centers in the high-k dielectric material. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that that make these limitations obvious. Claim 20, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 17 of the Office Action claim 23 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, and further in view of Chooi (US 6,486,080) and Agarwal (US 2001/0015453). The Office Action acknowledges that Halliyal does not describe a densification annealing, but that Chooi and Agarwal do. The

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Office Action states that it would have been obvious to follow the deposition of Halliyal's trapping layer with an annealing to cure oxygen vacancies. This rejection is traversed as follows.

At col. 6, ln 5-7, Chooi describes the densification of a metal oxide. At paragraph [0005] Agarwal describes densification to cure oxygen vacancies in a high-k dielectric. It is not clear how these references have any application to the claim invention, which performs a densification annealing to prevent delamination of the gate (specification, page 12, ln. 24-25). Further, neither of these references describes ion implantation processes, the use of a high-k dielectric as a charge trapping material, or the use of a high-k dielectric memory device. Rather, it appears as if the various references have been assembled as the result of a retrospective search, using the limitations of claim 23 as keywords. These references do not suggest any modifications to Tiwari's ion implantation of a low-k dielectric film. Likewise, these references do not suggest modifications to Halliyal's high-k dielectric reduction protection process.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. As noted above, Applicant's claim 16 recites a memory device formed through the steps of exposing a high-k material to an ionized species; and, in response to the ionized species exposure, inducing charge trapping centers in the high-k dielectric material. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that that make these limitations obvious. Claim 23, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

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In Section 19 of the Office Action claim 24 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, and further in view of Liang (US 65,372,957). The Office Action acknowledges that Halliyal does not describe a drain/source angle implant, as described by Liang. The Office Action states that it would have been obvious to form Halliyal's source/drain regions using Liang's process, to protect the transistor from hot carrier degradation. This rejection is traversed as follows.

Even if Liang does describe an angle implant to form source/drain regions, it is not apparent that Liang suggests any modifications to a process that ion implants a low-k dielectric (Tiwari), or to Halliyal's high-k dielectric reduction protection process.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. As noted above, Applicant's claim 16 recites a memory device formed through the steps of exposing a high-k material to an ionized species; and, in response to the ionized species exposure, inducing charge trapping centers in the high-k dielectric material. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that that make these limitations obvious. Claim 24, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

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It is believed that the application is in condition for allowance and reconsideration is earnestly solicited.

Respectfully submitted,

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